III. AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Previously Presented) A method for modeling a behavior of an LPAR (logical partition) in a simulated computer operating in a time slice dispatch mode, comprising:

beginning a modeling interval;

calculating a resource percentage representing a percentage of total resources allocated to the LPAR, wherein the resource percentage is equal to: 100% - a percentage of resources allocated to all other LPARs running in the simulated computer;

calculating a time slice percentage for the LPAR based on the resource percentage and CP (central processor) data, wherein:

time slice percentage = (resource percentage) x (# of physical CPs)
(# of logical CPs);

determining a CP (central processor) percentage representing a percentage of time that all physical CPs in the computer being modeled have been allocated to the LPAR;

if the CP percentage is greater than the time slice percentage, causing the simulated computer not to dispatch CPs to the LPAR; and

outputting and displaying the behavior of the modeling.

2. (Original) The method of claim 1, including the further step of repeating each of the recited steps for a next modeling interval.

3. (Cancelled).

4. (Previously Presented) The method of claim 1, wherein the percentage of resources allocated to all other LPARs is based on a weighting factor specified for each LPAR, a number of logical CPs allocated to each LPAR, and a MIPs (million instructions per second) value for each LPAR.

5. (Original) The method of claim 4, wherein the MIPs value represents a maximum consumption that each LPAR could consume in an unrestrained processor.

6. (Cancelled).

Claims 7-22. (Cancelled).